IN THE CLAIMS:

Claims 1 and 4 have been amended, as follows:

1. (currently amended) A bi-directional boost circuit for power factor correction, comprising:

a first diode, a second diode, a first inductor, a second inductor, a first switch, and a second switch to convert an AC input voltage, rectify the AC input voltage, and output an intermediate DC voltage; and

a power factor control circuit, the power factor circuit including

a waveform generator to receive the AC input voltage and generate a haversign waveform;

a pulse width modulator to generate a pulsed signal based on the intermediate DC voltage;

a multiplier to multiply the haversign waveform and the pulsed signal and to create a multiplied haversign signal;

an integrator to strip off high frequency characteristics of the multiplied haversign signal to create a haversign signal;

a first control circuit to compare a magnitude of the haversign signal ~~is compared~~ to a magnitude of [[the]] a first inductor current to generate a first drive signal; and

a second control circuit to compare a magnitude of the haversign signal to a magnitude of [[the]] a second inductor current to generate a second drive signal, which controls an inductor current waveform to form a substantially sinusoidal waveform that is in phase with the AC input voltage.

2. (original) The circuit of claim 1, wherein the power factor control circuit creates a clipped inductor current waveform if the power factor control circuit is

configured with a clipping threshold value and a value of an inductor current is above the clipping threshold value.

3. (previously presented) The circuit of claim 1, wherein the first control circuit is a first current mode controller and the second control circuit is a second current mode controller.

4. (currently amended) The circuit of claim 1, further including an error amplifier [[to]] to compare a reference voltage and the intermediate DC voltage and to generate an error signal and to input the error signal to the pulse width modulator to control a pulse width of the pulsed signal.

5. (previously presented) The circuit of claim 1, further including a comparator to clamp the haversign signal in response to a large instantaneous change in the intermediate DC output voltage.

Claims 6 – 8 (cancelled).

Claims 9 – 13 (cancelled).

14. (previously presented) A method of power factor correction, comprising:

receiving an AC input voltage;

generating an intermediate DC voltage;

generating, at a waveform generator, a haversign waveform;

generating a pulsed signal based on the intermediate DC voltage;

multiplying the haversign waveform and the pulsed signal to create a multiplied haversign signal;

stripping off high frequency characteristics of the multiplied haversign signal to create a haversign signal;

receiving a first inductor current through a first switch;

comparing a magnitude of the haversign signal with a value of the first inductor current; and

generating a first driving signal to turn off the first switch if the value of the first inductor current is larger than the magnitude of the haversign signal.

Claim 15 (cancelled).

16. (previously presented) The method of claim 14, further including

receiving a second inductor current through a second switch;

comparing a magnitude of the haversign signal with a value of the second inductor current; and

generating a second driving signal to turn off the second switch if the value of the second inductor current is larger than the magnitude of the haversign signal.

17. (original) The method of claim 16, further including,

receiving the AC input voltage at a first inductor and a second inductor;

rectifying the AC input voltage using the first switch, the second switch, a first diode, and a second diode to produce an intermediate DC voltage.

18. (previously presented) A method of power factor correction, comprising:

receiving an AC input voltage;

generating an intermediate DC voltage;

generating, at a waveform generator, a haversign waveform;

generating a pulsed signal based on the intermediate DC voltage;

multiplying the haversign waveform and the pulsed signal to create a multiplied haversign signal;

stripping off high frequency characteristics of the multiplied haversign signal to create a haversign signal;

receiving a first inductor current through a first switch;

comparing a clipping threshold value with a value of the first inductor current; and

generating a first driving signal to turn off the first switch if the value of the first inductor current is larger than the magnitude of the clipping threshold value.

19. (original) The method of claim 18, further including,

receiving a second inductor current through a second switch;

comparing the clipping threshold value with a value of the second inductor current; and

generating a second driving signal to turn off the second switch if the value of the second inductor current is larger than the clipping threshold value.

20. (original) The method of claim 19, further including,

receiving the AC input voltage at a first inductor and a second inductor;

rectifying the AC input voltage using the first switch, the second switch, a first diode, and a second diode to produce an intermediate DC voltage.

Claims 21 – 37 (cancelled).